ALPHA DATA

ADC-XMC-II

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1 About the Hardware

The ADC-XMC-II is a full length PCI Express card design to carry two Switched Mezzanine Cards (XMCs). The card can be used in x1, x2, x4 and x8 PCIe Gen 1 or 2 signaling environments installed in x8 or x16 PCIe slot. The two XMC sites on the card support up to one x8 PCIe Gen 2 or up to two x4 PCIe Gen 2 links (lower link widths are also support). VPWR provided to the XMC cards is set at 12V.

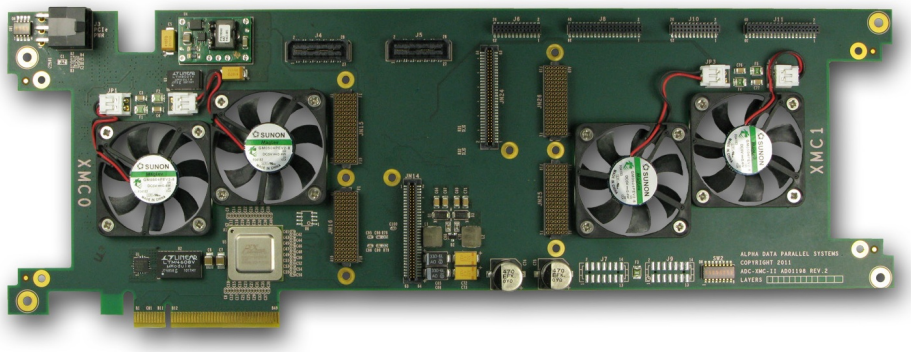

Figure 1: ADC-XMC-II Photo

1.1 XMC Architecture

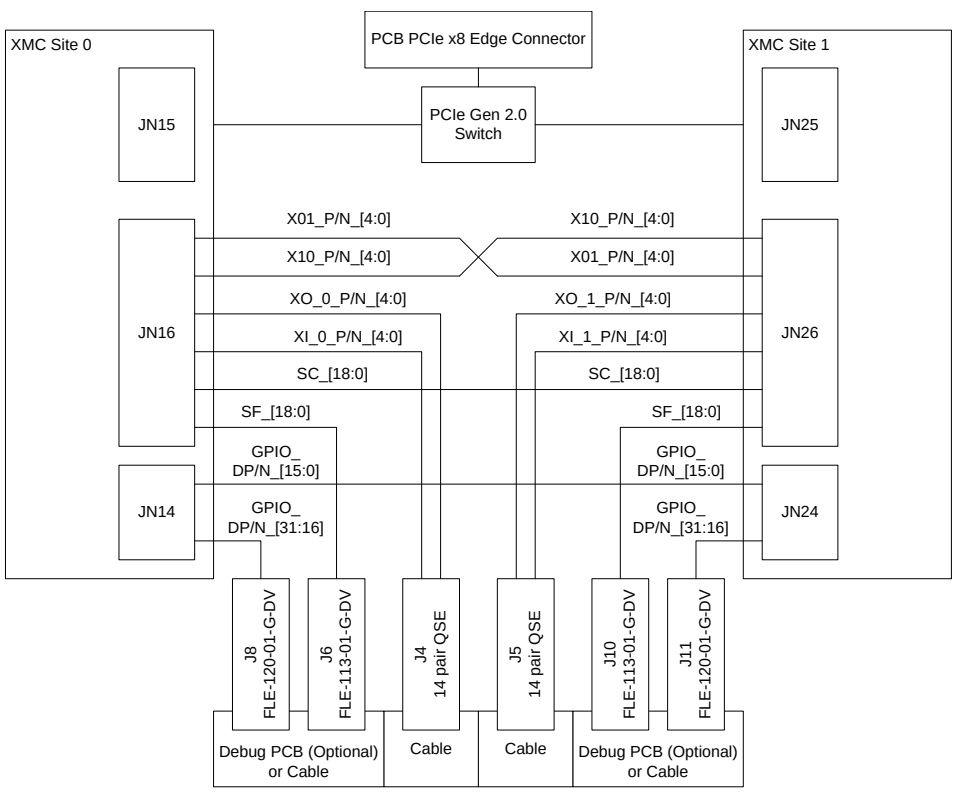

Figure 2: ADC-XMC-II Conectivity

1.2 Board Features

The following photos highlight the various features of the ADC-XMC-II.

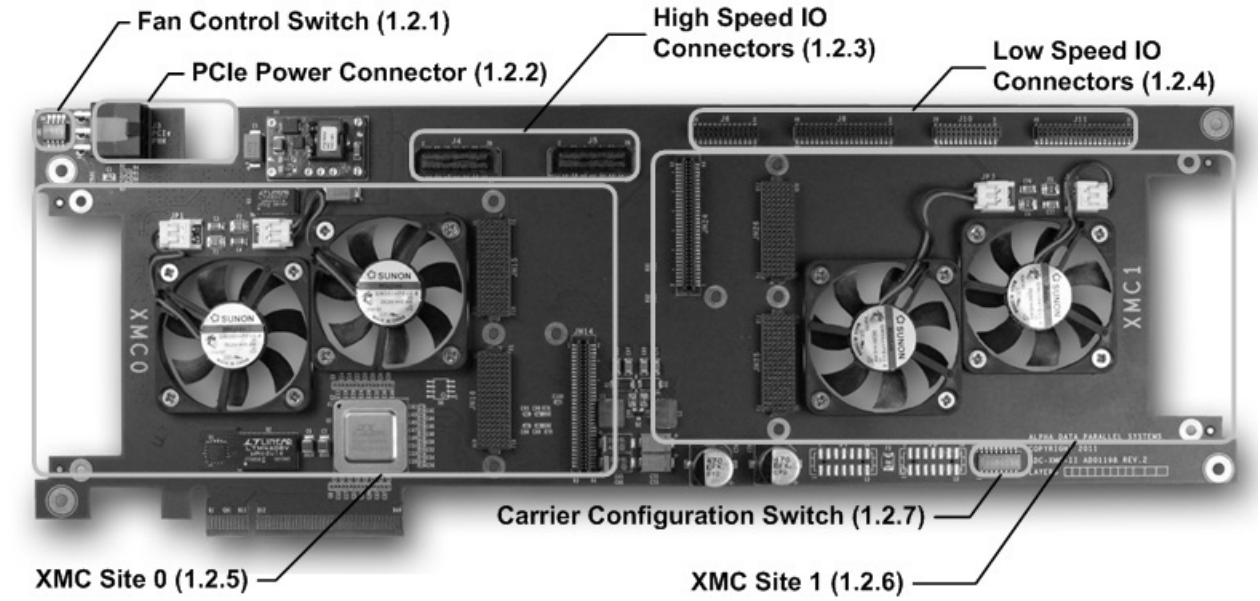

Figure 3: Features Front

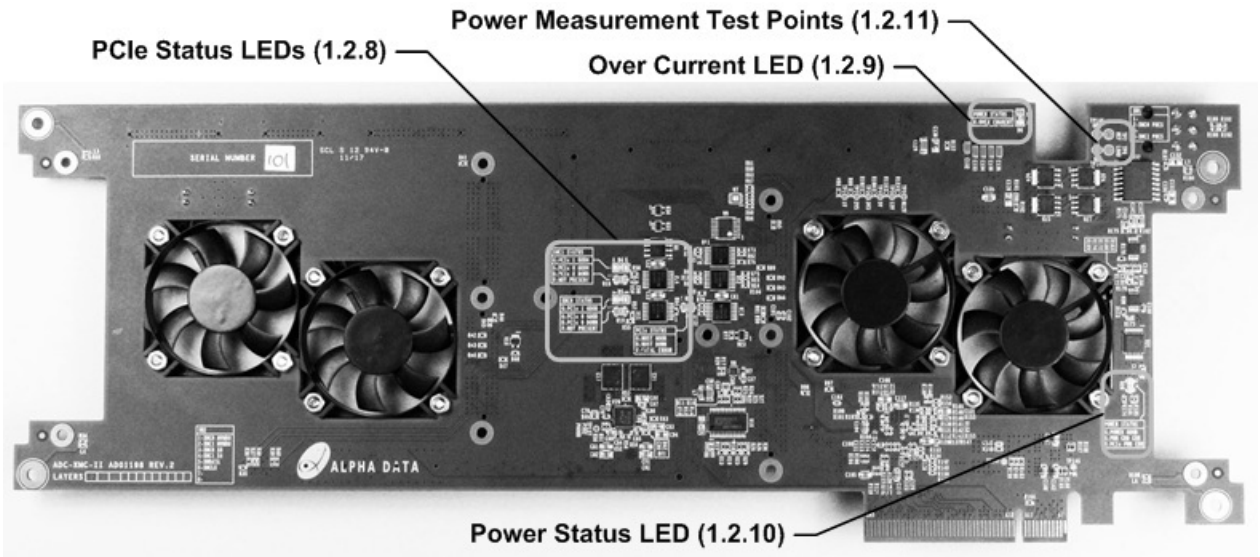

Figure 4: Features Back

The following subsections each detail the highlighted features.

1.2.1 Fan Control Switch (SW1)

This set of switches can be used to force fans to turn on at each XMC site. All reserved switches must be set to their default position.

Switch	Off Position	On Position
1	Reserved (Default)	Reserved
2	Fans for XMC Site 0 are controlled by XMC 0 MPRS# (J15, pin F14)	Forces fans for XMC Site 0 on. (Default)
3	Reserved (Default)	Reserved
4	Fans for XMC Site 1 are controlled by XMC 1 MPRS# (J25, pin F14)	Forces fans for XMC Site 1 on. (Default)

Table 1: SW1

1.2.2 PCIe Power Connector

This connector should be connected to the system's power supply using a standard 6-pin PCIe power cable.

1.2.3 High Speed IO Connectors (J4,J5)

These connectors allow high speed serial IO (HSSIO) connections to XO_0/1_P/N_[4:0] (TX) and XI_0/1_P/N_[4:0] (RX). The connectors and tracking to XMC sites is suitable for speeds upto 5Gb/s.

1.2.4 Low Speed IO Connectors (J6/J10 and J8/J11)

These connectors allow lower speed IO connections to the single ended IO SF_[18:0], suitable for signals up to 600 Mb/s, and GPIO_DP/N_[31:16], suitable for signals up to 1 Gb/s.

1.2.5 XMC Site 0

An XMC card may be fitted here with its IO area accessable externally though the rear panel.

1.2.6 XMC Site 1

An XMC card may be fitted here with its IO area accessable internally.

1.2.7 Carrier Configuration Switch (SW2)

This set of switches is used to configure the ADC-XMC-II. All reserved switches must be set to their default position.

Switch	Off Position	On Position
1	XMC Site 0 MVMRO (J15, pin C16) pulled low (Default)	XMC Site 0 MVMRO (J15, pin C16) pulled high
1	XMC Site 1 MVMRO (J25, pin C16) pulled low (Default)	XMC Site 1 MVMRO (J25, pin C16) pulled high
3	XMC Site 0 PCIe is configured for two x4 Gen 2 PCIe links (Default)	XMC Site 0 PCIe is configured for one x8 Gen 2 PCIe link
4	XMC Site 1 PCIe is configured for one x8 Gen 2 PCIe link	XMC Site 1 PCIe is configured for two x4 Gen 2 PCIe links (Default)
5	Reserved (Default)	Reserved
6	Reserved (Default)	Reserved
7	Reserved (Default)	Reserved
8	Reserved (Default)	Reserved

Table 2: SW2

1.2.8 PCIe Status LEDs

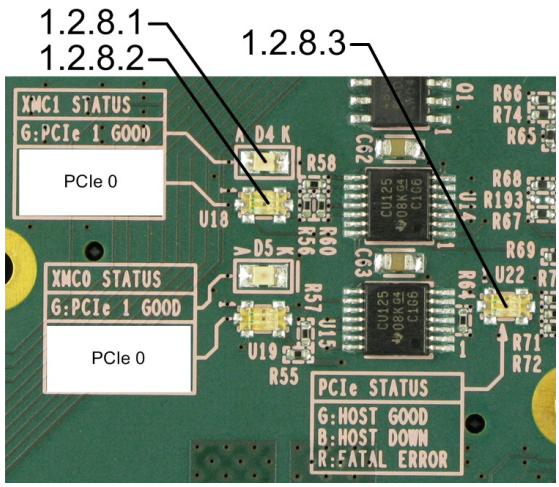

Figure 5: PCIe Status LEDs

1.2.8.1 XMC 0/1 PCIe 1 Status

This green LED (locatated above each tri-colour LED) indicate when the second x4 link is up if the ADC-XMC-II is configured for two x4 links to an XMC site.

1.2.8.2 XMC 0/1 PCIe 0 Status

This tri-colour LED indicates the status of the primary PCIe link to the an XMC site.

Green: ADC-XMC-II is running a x8 Gen 2 connection to the host; or x4 Gen 2 if configured for two x4 links.

Flashing Red/Green: ADC-XMC-II is running a x4 Gen 2 (or less) connection to the host; if in two x4 mode it indicate ADC-XMC is running less than a x4 or slower than Gen 2 on the first PCIe link to the site.

Red: PCIe Link down.

Blue: XMC card not present.

1.2.8.3 Host Link PCIe Status

This tri-colour LED indicates the status of the PCIe link to the host.

Green: ADC-XMC-II is running a x8 Gen 2 connection to the host.

Flashing Blue/Green: ADC-XMC-II is running a x4 Gen 1 or 2 connection to the host.

Blue: Host PCIe link is down.

Red: Fatal PCIe fault.

1.2.9 Overcurrent LED

When illumanated this LED (red) indicates that more than 75W is being drawn.

1.2.10 Power Status LED

Always illuminated in one of three colours.

Green: indicates 12V is being provided from the PCIe edge connector, and also the 6-pin PCIe power connector (normal operation).

Blue: indicates 12V is being provided from the PCIe edge connector, but not the 6-pin PCIe power connector (low power operation).

Red: indicates 12V is being provided via the 6-pin PCIe power connector, but not the PCIe edge connector.

Off: indicates card has no power.

1.3 Power Measurement Test Points

Two test points are provided TP7 and TP8 that can be used to measure the power being consumed by the card. See **Section 1.5.2, "Measuring power"** for more information.

1.4 Installation

In order to ensure that the board operates correctly first time, please read these instructions completely before attempting installation. It will also help you to read the whole manual first so that you know how you want the board to be set up.

The ADC-XMC-II can be installed in a x8 or x16 PCIe slot.

- Fit any XMC modules that are required.
- If only one XMC module is to be fitted, either site can be used.
- XMC site 0 is positioned so that an I/O connector on the module aligns with the aperture in the ADC-EMC's edge panel.
- The XMC modules should be supplied with mounting kits, which normally include spacers, nuts, bolts and washers.

No software is required to enable operation of the ADC-XMC-II.

1.5 Power

The ADC-XMC-II is designed to support standard XMCs, and their power requirements. However, a total of 75W should not exceeded (including the power dissipated by the carrier itself).

1.5.1 Requirements

The ADC-XMC-II can operate using the power provided by the PCI Express edge connector if the XMC cards require less than 25W total. It is recommend that the 6 pin PCIe power connector be connected to allow a connection to the system power supply to source up to 75W (12V at up to 6.25A).

Note: The ADC-XMC-II should be used in a system with a ATX12V v2.1 (or compatible) power supply.

1.5.2 Measuring power

The ADC-XMC-II has test points that can be used to measure power being consumed TP7 and TP8. This measurement as well as including the power dissipation by the XMCs also includes the power dissipated by the fans, control logic, and LEDs on the ADC-XMC-II. The measure excludes the power dissipated by the PCIe switch on the ADC-XMC-II.

When measuring power, ~6.2W should be subtracted from the total measured to calculate the power usage of attached cards. To increase the accuracy of the measurement one reading should be taken with no cards attached (but the required fans for intended application forced to be running using SW1). Then a second reading should be taken with XMC cards attached and the system running the desired appliction. The difference between the values is the amount of power being consumed by the XMCs.

1.5.2.1 Calculation

The following formula should be used to convert the measued voltages at testpoint TP8 and TP7 (in Volts) into the power consumed in Watts.

Power Consumption = (((TP8 - TP7) / 0.056) x 12)

1.5.2.2 Limits

Supply	Limit	Unit
Total Power (with XMC cards)	75.0	W
Max. Required Carrier Power	9.62	W
M12V (per XMC site)	1	A
3V3 (per XMC site)	4	A
3V3 Aux (per XMC site)	1	A
VPWR (12V) (per XMC site)	8	A
12V (per XMC site)	1	A

Table 3: Supply Limits

1.6 Cables

This section details recommended cables for interconnection of ADC-XMC-II carrier cards.

1.6.1 Single End and Differential IO (J6,J10,J8,J11)

The cables recommend below for interconnection boards have a 1-1 mapping. It maybe more appropriate to a developer to use a different mapping to suit their appliction.

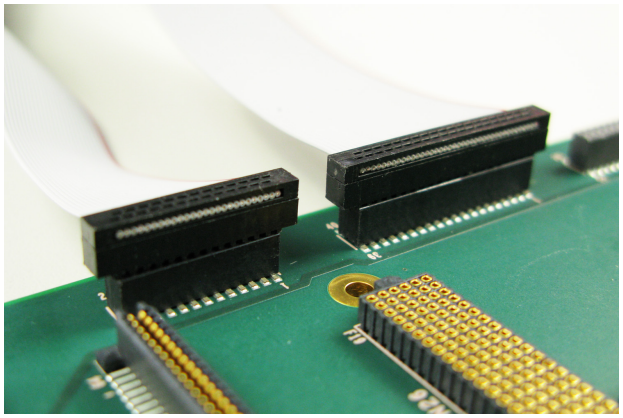

Figure 6: Low Speed Cables (J6/J10 and J8/J11)

J6/J10: Samtec FFMD-13-D-08.00-01-R

J8/J11: Samtec FFMD-20-D-08.00-01-R

1.6.2 HSSIO (J4,J5)

The cable recommended below for interconnection of high speed serial IO (HSSIO) has a 1-2 mapping (swapping the RX lanes with the TX lanes in the cable between carriers giving the required TX to RX connectivity).

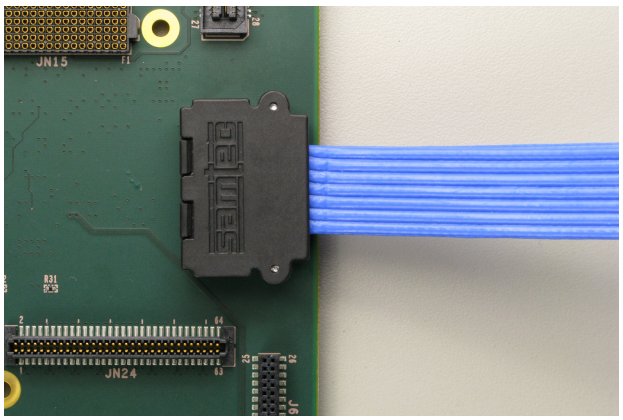

Figure 7: High Speed Cable (J4/J5)

J4/J5: Samtec EQDP-014-08.00-TTR-TBL-2

2 Connector Pinout

2.1 J8/J11

Pin	Name	Pin	Name
1	GND	2	GND
3	GPIO_x_DP_16	4	GPIO_x_DN_16
5	GPIO_x_DP_17	6	GPIO_x_DN_17
7	GPIO_x_DP_18	8	GPIO_x_DN_18
9	GPIO_x_DP_19	10	GPIO_x_DN_19
11	GPIO_x_DP_20	12	GPIO_x_DN_20
13	GPIO_x_DP_21	14	GPIO_x_DN_21
15	GPIO_x_DP_22	16	GPIO_x_DN_22
17	GPIO_x_DP_23	18	GPIO_x_DN_23
19	GND	20	GND
21	GND	22	GND
23	GPIO_x_DP_24	24	GPIO_x_DN_24
25	GPIO_x_DP_25	26	GPIO_x_DN_25
27	GPIO_x_DP_26	28	GPIO_x_DN_26
29	GPIO_x_DP_27	30	GPIO_x_DN_27
31	GPIO_x_DP_28	32	GPIO_x_DN_28
33	GPIO_x_DP_29	34	GPIO_x_DN_29
35	GPIO_x_DP_30	36	GPIO_x_DN_30
37	GPIO_x_DP_31	38	GPIO_x_DN_31
39	GND	40	GND

Table 4: Differential GPIO Pinout (ADC-XMC-II)

2.2 J6/J10

Pin	Name	Pin	Name
1	GND	2	GND
3	SF_0	4	SF_1
5	SF_2	6	SF_3
7	SF_4	8	SF_5
9	SF_6	10	SF_7
11	SF_8	12	SF_9
13	GND	14	GND
15	SF_10	16	SF_11
17	SF_12	18	SF_13
19	SF_14	20	SF_15
21	SF_16	22	SF_17
23	SF_18	24	
25	GND	26	GND

Table 5: Singed Ended GPIO Pinout (ADC-XMC-II)

2.3 J4/J5

Pin	Name	Pin	Name
1	XO_n_P_0	2	XI_n_P_0
3	XO_n_N_0	4	XI_n_N_0
5	XO_n_P_1	6	XI_n_P_1
7	XO_n_N_1	8	XI_n_N_1
9	GND	10	GND
11	GND	12	GND
13	XO_n_P_4	14	XI_n_P_4
15	XO_n_N_4	16	XI_n_N_4
17	GND	18	GND
19	GND	20	GND
21	XO_n_P_2	22	XI_n_P_2
23	XO_n_N_2	24	XI_n_N_2
25	XO_n_P_3	26	XI_n_P_3
27	XO_n_N_3	28	XI_n_N_3

Table 6: High Speed Serial IO Pinout (ADC-XMC-II)

2.4 J14/J24

Pin	Name	Pin	Name
1	GPIO_x_DP_0	2	GPIO_x_DP_16
3	GPIO_x_DN_0	4	GPIO_x_DN_16
5	GPIO_x_DP_1	6	GPIO_x_DP_17
7	GPIO_x_DN_1	8	GPIO_x_DN_17
9	GPIO_x_DP_2	10	GPIO_x_DP_18
11	GPIO_x_DN_2	12	GPIO_x_DN_18
13	GPIO_x_DP_3	14	GPIO_x_DP_19
15	GPIO_x_DN_3	16	GPIO_x_DN_19
17	GPIO_x_DP_4	18	GPIO_x_DP_20
19	GPIO_x_DN_4	20	GPIO_x_DN_20
21	GPIO_x_DP_5	22	GPIO_x_DP_21
23	GPIO_x_DN_5	24	GPIO_x_DN_21
25	GPIO_x_DP_6	26	GPIO_x_DP_22
27	GPIO_x_DN_6	28	GPIO_x_DN_22
29	GPIO_x_DP_7	30	GPIO_x_DP_23
31	GPIO_x_DN_7	32	GPIO_x_DN_23
33	GPIO_x_DP_8	34	GPIO_x_DP_24
35	GPIO_x_DN_8	36	GPIO_x_DN_24
37	GPIO_x_DP_9	38	GPIO_x_DP_25
39	GPIO_x_DN_9	40	GPIO_x_DN_25
41	GPIO_x_DP_10	42	GPIO_x_DP_26
43	GPIO_x_DN_10	44	GPIO_x_DN_26
45	GPIO_x_DP_11	46	GPIO_x_DP_27
47	GPIO_x_DN_11	48	GPIO_x_DN_27
49	GPIO_x_DP_12	50	GPIO_x_DP_28
51	GPIO_x_DN_12	52	GPIO_x_DN_28
53	GPIO_x_DP_13	54	GPIO_x_DP_29
55	GPIO_x_DN_13	56	GPIO_x_DN_29
57	GPIO_x_DP_14	58	GPIO_x_DP_30
59	GPIO_x_DN_14	60	GPIO_x_DN_30
61	GPIO_x_DP_15	62	GPIO_x_DP_31
63	GPIO_x_DN_15	64	GPIO_x_DN_31

Table 7: Jn4 Pinout (ADC-XMC-II)

2.5 J15/J25

Pin	Net	Pin	Net	Pin	Net	Pin	Net	Pin	Net	Pin	Net
A1	PET0p0	B1	PET0n0	C1	3V3	D1	PET0p1	E1	PET0n1	F1	12V
A2	GND	B2	GND	C2	TRST	D2	GND	E2	GND	F2	MRSTI#
A3	PET0p2	B3	PET0n2	C3	3V3	D3	PET0p3	E3	PET0n3	F3	12V
A4	GND	B4	GND	C4	TCK	D4	GND	E4	GND	F4	-
A5	PET0p4	B5	PET0n4	C5	3V3	D5	PET0p5	E5	PET0n5	F5	12V
A6	GND	B6	GND	C6	TMS	D6	GND	E6	GND	F6	12V
A7	PET0p6	B7	PET0n6	C7	3V3	D7	PET0p7	E7	PET0n7	F7	12V
A8	GND	B8	GND	C8	TDI	D8	GND	E8	GND	F8	M12V
A9	-	B9	-	C9	-	D9	-	E9	-	F9	12V
A10	GND	B10	GND	C10	TDO	D10	GND	E10	GND	F10	GA0
A11	PER0p0	B11	PER0n0	C11	-	D11	PER0p1	E11	PER0n1	F11	12V
A12	GND	B12	GND	C12	GA1	D12	GND	E12	GND	F12	MPRS#
A13	PER0p2	B13	PER0n2	C13	3V3 Aux	D13	PER0p3	E13	PER0n3	F13	12V
A14	GND	B14	GND	C14	GA2	D14	GND	E14	GND	F14	MSDA
A15	PER0p4	B15	PER0n4	C15	-	D15	PER0p5	E15	PER0n5	F15	12V
A16	GND	B16	GND	C16	MVMRO	D16	GND	E16	GND	F16	MSCL
A17	PER0p6	B17	PER0n6	C17	-	D17	PER0p7	E17	PER0n7	F17	-
A18	GND	B18	GND	C18	-	D18	GND	E18	GND	F18	-
A19	REF_CLK_P	B19	REF_CLK_N	C19	-	D19	WAKE_L	E19	ROOT_L	F19	-

Table 8: Jn5 Pinout (ADC-XMC-II)

2.6 J16/J26

Pin	Net	Pin	Net	Pin	Net	Pin	Net	Pin	Net	Pin	Net
A1	X01_P_0	B1	X01_N_0	C1	SC_0	D1	X01_P_1	E1	X01_N_1	F1	SF_0
A2	GND	B2	GND	C2	SC_1	D2	GND	E2	GND	F2	SF_1
A3	X01_P_2	B3	X01_N_2	C3	SC_2	D3	X01_P_3	E3	X01_N_3	F3	SF_2
A4	GND	B4	GND	C4	SC_3	D4	GND	E4	GND	F4	SF_3
A5	XO_0_P_0	B5	XO_0_N_0	C5	SC_4	D5	XO_0_P_1	E5	XO_0_N_1	F5	SF_4
A6	GND	B6	GND	C6	SC_5	D6	GND	E6	GND	F6	SF_5
A7	XO_0_P_2	B7	XO_0_N_2	C7	SC_6	D7	XO_0_P_3	E7	XO_0_N_3	F7	SF_6
A8	GND	B8	GND	C8	SC_7	D8	GND	E8	GND	F8	SF_7
A9	X01_P_4	B9	X01_N_4	C9	SC_8	D9	XO_0_P_4	E9	XO_0_N_4	F9	SF_8
A10	GND	B10	GND	C10	SC_9	D10	GND	E10	GND	F10	SF_9
A11	X10_P_0	B11	X10_N_0	C11	SC_10	D11	X10_P_1	E11	X10_N_1	F11	SF_10
A12	GND	B12	GND	C12	SC_11	D12	GND	E12	GND	F12	SF_11
A13	X10_P_2	B13	X10_N_2	C13	SC_12	D13	X10_P_3	E13	X10_N_3	F13	SF_12
A14	GND	B14	GND	C14	SC_13	D14	GND	E14	GND	F14	SF_13
A15	XI_0_P_0	B15	XI_0_N_0	C15	SC_14	D15	XI_0_P_1	E15	XI_0_N_1	F15	SF_14
A16	GND	B16	GND	C16	SC_15	D16	GND	E16	GND	F16	SF_15
A17	XI_0_P_2	B17	XI_0_N_2	C17	SC_16	D17	XI_0_P_3	E17	XI_0_N_3	F17	SF_16
A18	GND	B18	GND	C18	SC_17	D18	GND	E18	GND	F18	SF_17
A19	X10_P_4	B19	X10_N_4	C19	SC_18	D19	XI_0_P_4	E19	XI_0_N_4	F19	SF_18

Table 9: Jn6 Pinout (ADC-XMC-II)

3 Debug PCB

A debug PCB is available that can be attached directly onto the low speed IO connectors. The thru hole terminals provided have a 2.54mm pitch. One of these debug PCBs is provided with each carrier. Developers should solder desired connections directly to the debug PCB. Additional debug PCBs may be ordered from Alpha Data.

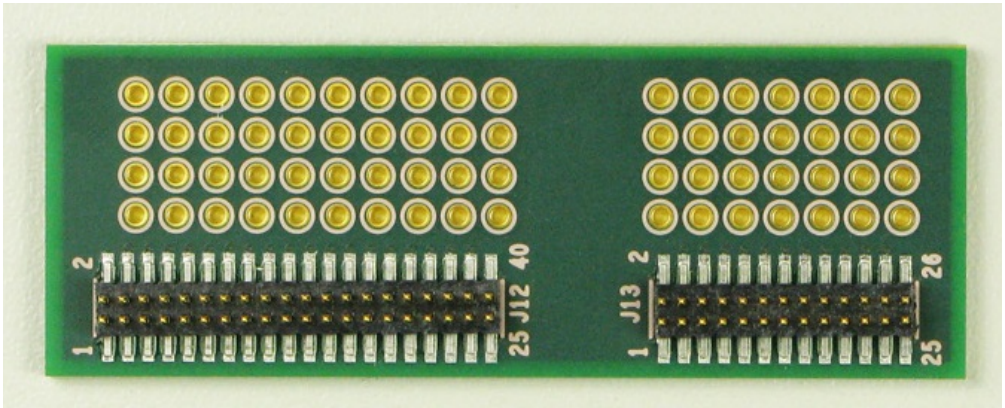

Figure 8: Debug PCB photo (bottom)

All custom connections to the debug PCB should be fitted from the top side of the board (where only one pin in each of the two groups is marked with an addiitonal circle round it). Connections should be soldered on the bottom side of the board (the side with the connectors that mate with the ADC-XMC-II).

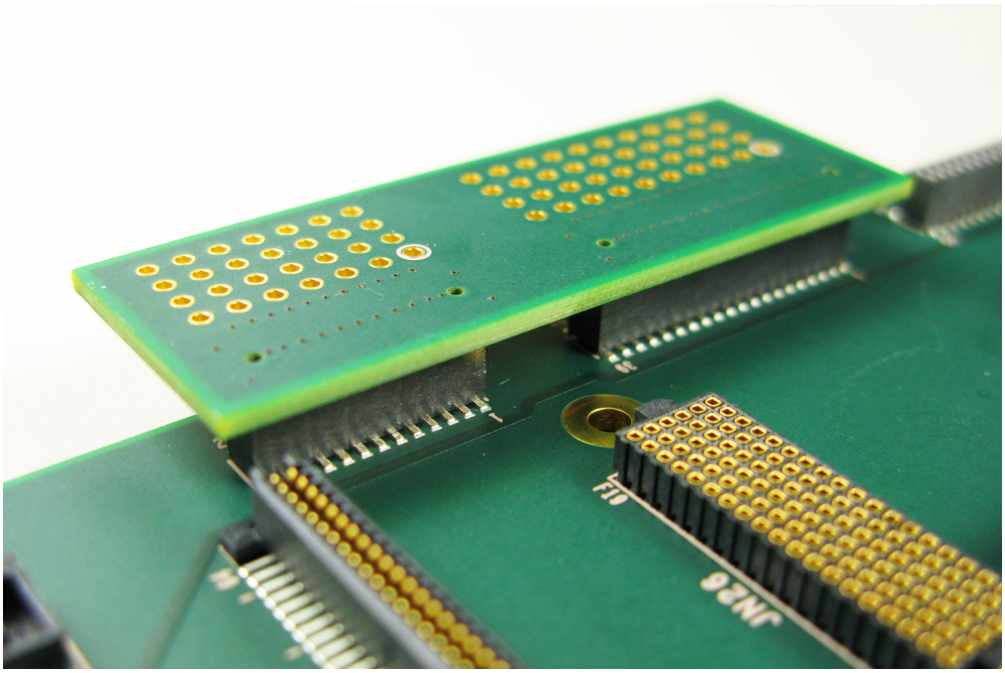

Figure 9: Test board fitted

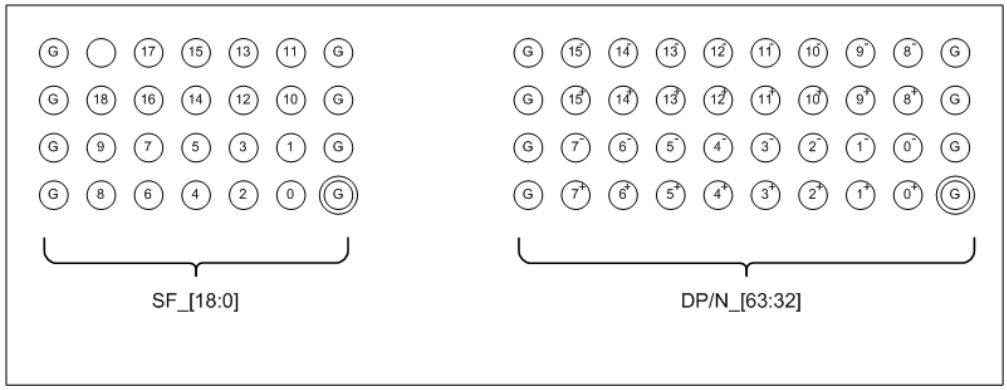

Figure 10: Debug PCB diagram (top)

The following table details the bus connections of each terminal labelled in the image above.

Pin	Name	Pin	Name
0	SF_0	1	SF_1
2	SF_2	3	SF_3
4	SF_4	5	SF_5
6	SF_6	7	SF_7
8	SF_7	9	SF_9
10	SF_10	11	SF_11
12	SF_12	13	SF_13
14	SF_14	15	SF_15
16	SF_16	17	SF_17
18	SF_18		
0+	GPIO_x_DP_16	0-	GPIO_x_DN_16
1+	GPIO_x_DP_17	1-	GPIO_x_DN_17
2+	GPIO_x_DP_18	2-	GPIO_x_DN_18
3+	GPIO_x_DP_19	3-	GPIO_x_DN_19
4+	GPIO_x_DP_20	4-	GPIO_x_DN_20
5+	GPIO_x_DP_21	5-	GPIO_x_DN_21
6+	GPIO_x_DP_22	6-	GPIO_x_DN_22
7+	GPIO_x_DP_23	7-	GPIO_x_DN_23
8+	GPIO_x_DP_24	8-	GPIO_x_DN_24
9+	GPIO_x_DP_25	9-	GPIO_x_DN_25
10+	GPIO_x_DP_26	10-	GPIO_x_DN_26
11+	GPIO_x_DP_27	11-	GPIO_x_DN_27
12+	GPIO_x_DP_28	12-	GPIO_x_DN_28
13+	GPIO_x_DP_29	13-	GPIO_x_DN_29
14+	GPIO_x_DP_30	14-	GPIO_x_DN_30
15+	GPIO_x_DP_31	15-	GPIO_x_DN_31

Table 10: Debug PCB Pinout

4 References and Specifications

ANSI/VITA 42.0 XMC Standard, December 2008, VITA, ISBN 1-885731-49-3

ANSI/VITA 42.3 XMC PCI Express Protocol Layer Standard, June 2006, VITA, ISBN 1-885731-43-4

ANSI/IEEE 1386-2001 IEEE Standard for a Common Mezzanine Card (CMC) Family, October 2001, IEEE, ISBN 0-7381-2829-5

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Revision History:

Revision	Date	Description of Change
1.0	July-2011	First issued.

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